

DATA SHEET

TDA8040T Quadrature demodulator

Objective specification
Supersedes data of 1995 Feb 07
File under Integrated Circuits, IC02

1996 Oct 08

Quadrature demodulator

TDA8040T

FEATURES

- +5 V supply voltage
- Bandgap internal reference voltage
- Low crosstalk between I (in-phase) and Q (quadrature) channel outputs
- High operating input sensitivity
- High Carrier-to-Noise Ratio (CNR) of the VCO.

APPLICATIONS

- Quadrature Phase Shift Keying (QPSK) demodulation.

GENERAL DESCRIPTION

The TDA8040T is a monolithic bipolar IC dedicated for quadrature demodulation.

It has been designed to operate in conjunction with the TDA8041H to provide a complete QPSK demodulator.

The design of this circuit has been optimized to provide the best quadrature accuracy necessary for digital receiver applications and particularly for digital television.

The TDA8040T includes two matched mixers, an RF amplifier, a symmetrical Voltage Controlled Oscillator (VCO), a frequency divider and two matched amplifiers. Two external filters are required for the baseband filtering.

The VCO requires an external LC tank circuit with two varicap diodes. This oscillator operates at twice the IF carrier frequency and can be used in a carrier recovery AFC loop.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
$I_{CC(tot)}$	total supply current	$V_{CC} = 5\text{ V}$	70	79	90	mA
$V_{i(RF)}$	operating input voltage level		64	67	70	dB μ V
$f_{i(RF)}$	RF input signal frequency		10.7	–	150	MHz
$V_{oIQ(p-p)}$	I and Q output voltage (peak-to-peak value)		–	0.5	–	V
$E_{\phi(IQ)}$	phase error between the I and Q channels		–	–	3	deg
$E_{G(IQ)}$	gain error between the I and Q channels		–	–	1	dB
$E_{G(tilt)}$	gain tilt error in the I and Q channels		–	–	1	dB
$\alpha_{ct(IQ)}$	crosstalk between the I and Q channels		30	–	–	dB
IM3	intermodulation distortion in the I and Q channels		40	–	–	dB

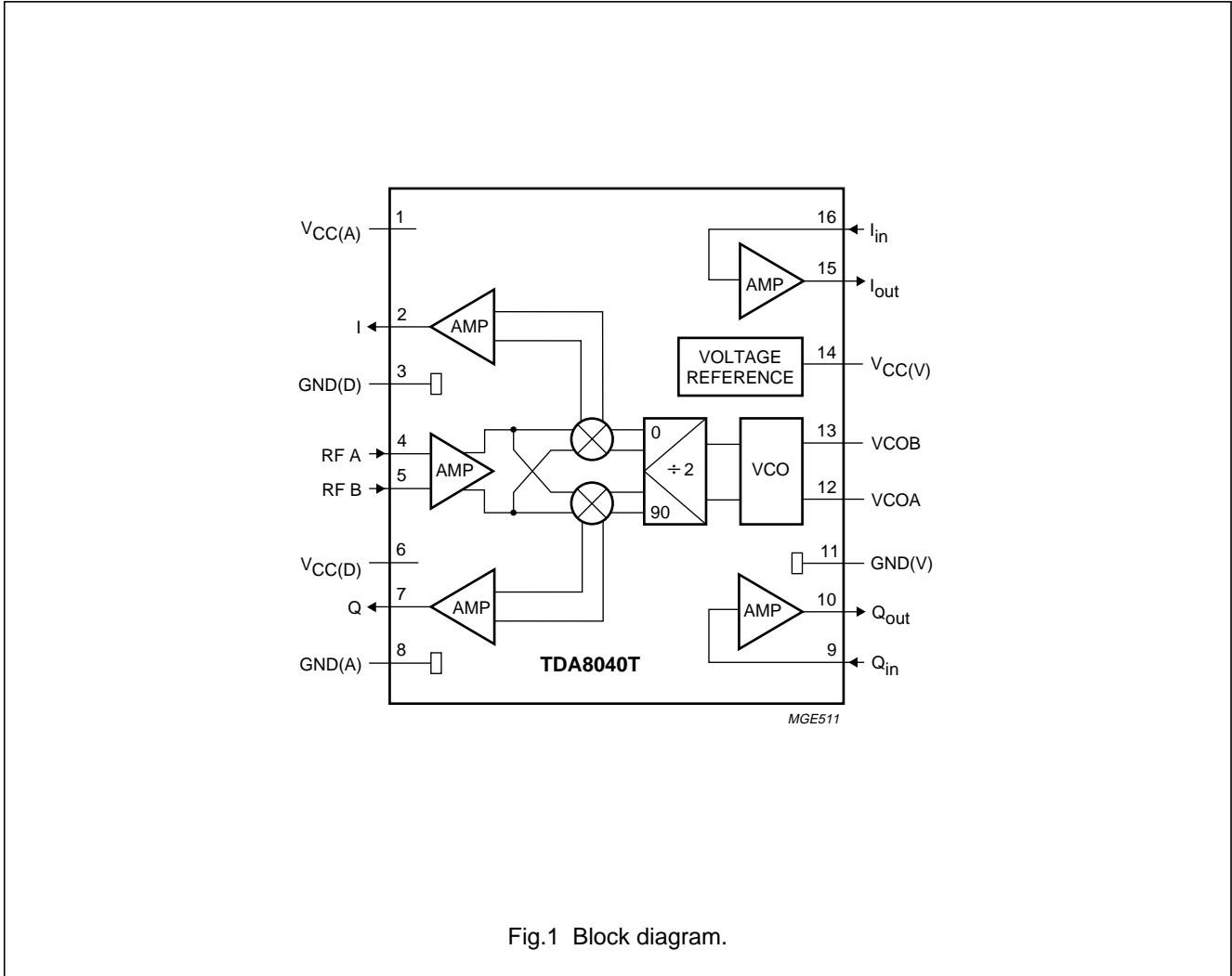
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8040T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

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BLOCK DIAGRAM



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PINNING

SYMBOL	PIN	DESCRIPTION
V _{CC(A)}	1	supply voltage for I and Q amplifiers
I	2	I channel buffer output
GND(D)	3	demodulator ground
RF A	4	RF input A
RF B	5	RF input B
V _{CC(D)}	6	supply voltage for demodulator
Q	7	Q channel buffer output
GND(A)	8	I and Q amplifiers ground
Q _{in}	9	Q channel amplifier input
Q _{out}	10	Q channel amplifier output
GND(V)	11	VCO ground
VCOA	12	VCO tank circuit A
VCOB	13	VCO tank circuit B
V _{CC(V)}	14	supply voltage for VCO
I _{out}	15	I channel amplifier output
I _{in}	16	I channel amplifier input

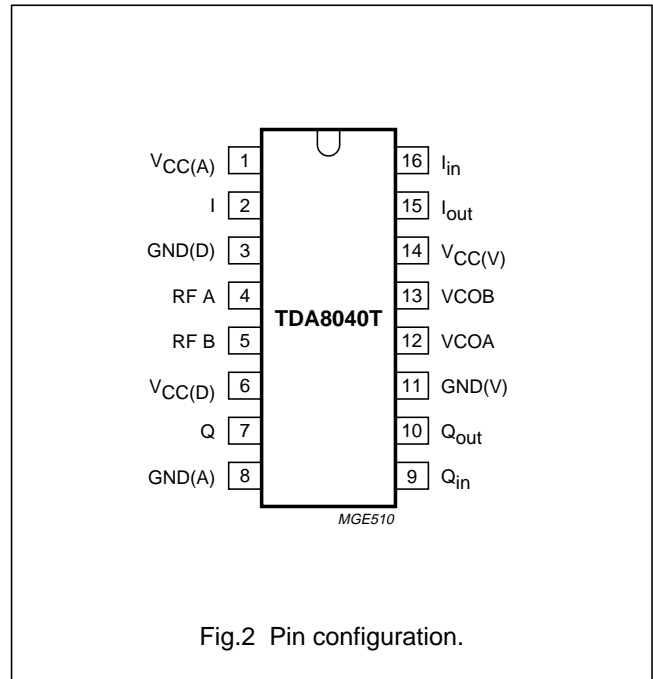


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The QPSK modulated RF signal is applied at the input of a high gain RF amplifier. The amplified signal is then mixed in a pair of mixers with two LO signals, which are 90 degrees out of phase, to produce the in-phase (I) and quadrature (Q) signals. These two signals are separately buffered to drive the external low-pass filters used for the baseband filtering. The I and Q signals are then amplified by two matched amplifiers designed to avoid crosstalk between channels.

The VCO operates at twice the carrier frequency. Its output signal is applied to a frequency divider (divide-by-2) to produce the two LO signals which are 90 degrees out of phase. The VCO is powered from the internal voltage stabilizer to ensure good shift performance.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC(A)}$	supply voltage for I and Q amplifiers		-0.3	+6.0	V
$V_{CC(D)}$	supply voltage for demodulator		-0.3	+6.0	V
$V_{CC(V)}$	supply voltage for VCO		-0.3	+6.0	V
$V_{n(max)}$	maximum voltage on all pins		-0.3	V_{CC}	V
I_{max}	maximum sink or source current		-	10	mA
$t_{sc(max)}$	maximum short-circuit time on outputs		-	10	s
$Z_{L(IQ)}$	AC load impedance for I and Q channels	$f_i = 15$ MHz	35	-	Ω
$Z_{LA(IQ)}$	AC load impedance for I and Q output amplifiers	$f_i = 15$ MHz	300	-	Ω
$V_{VCO(p-p)}$	voltage drive level for external oscillator signal (peak-to-peak value)		-	0.6	V
P_{tot}	total power dissipation	$T_{amb} = 70$ °C	-	500	mW
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-	150	°C
T_{amb}	operating ambient temperature		0	70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th j-a}$	thermal resistance from junction to ambient in free air	110	K/W

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CHARACTERISTICS

$V_{CC(A)} = V_{CC(D)} = V_{CC(V)} = 5\text{ V}$; $f_{i(RF)} = 70\text{ MHz}$; $f_{i(VCO)} = 140\text{ MHz}$; $V_{i(RF)} = 67\text{ dB}\mu\text{V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; measured in application circuit of Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{CC(A)}$	supply voltage for I and Q channel amplifier		4.75	5.0	5.25	V
$V_{CC(D)}$	supply voltage for demodulator		4.75	5.0	5.25	V
$V_{CC(V)}$	supply voltage for VCO		4.75	5.0	5.25	V
$I_{CC(A)}$	supply current for I and Q channel amplifier	note 1	–	29	–	mA
$I_{CC(D)}$	supply current for demodulator	note 1	–	16	–	mA
$I_{CC(V)}$	supply current for VCO	note 1	–	34	–	mA
QPSK demodulator						
$f_{i(RF)min}$	minimum input IF frequency		–	–	10.7	MHz
$f_{i(RF)max}$	maximum input IF frequency		150	–	–	MHz
$R_{i(RF)}$	resistive input impedance		–	50	–	Ω
$X_{i(RF)}$	reactive input impedance		–	5	–	Ω
$V_{i(RF)}$	operating input voltage		64	67	70	dB μ V
$R_{o(IQ)}$	output resistance for I and Q channels		45	50	55	Ω
$V_{oIQ(p-p)}$	output voltage for I and Q channels (peak-to-peak value)	note 2	–	85	–	mV
$G_{ch(IQ)}$	I and Q channel gain	note 3	21	22.5	24	dB
$E_{\phi(IQ)}$	phase error between I and Q channels	note 4	–	–	3	deg
$E_{G(IQ)}$	gain error between I and Q channels	note 4	–	–	0.5	dB
$E_{G(tilt)}$	gain tilt error between I and Q channels	note 5	–	–	0.8	dB
NF	double sideband noise figure	$Z_{source} = 50\ \Omega$; note 6	–	17	20	dB
IM3	intermodulation distortion in the I and Q channels	note 7	45	–	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator (VCO)						
$f_{iVCO(min)}$	minimum input oscillator frequency		–	–	21.4	MHz
$f_{iVCO(max)}$	maximum input oscillator frequency		300	–	–	MHz
Δf	frequency deviation		–	6	–	MHz
Δf_{drift}	frequency drift	note 8	–	–	100	kHz
Δf_{shift}	frequency shift	$\Delta V_{CC} = 5\%$	–	–	100	kHz
CNR_{osc}	oscillator carrier-to-noise ratio	at 10 kHz; note 9	–	85	–	dBc/Hz
		at 100 kHz; note 9	–	105	–	dBc/Hz
$V_{osc(p-p)}$	required voltage drive level for external oscillator injection (peak-to-peak value)		100	–	–	mV
$R_{source(osc)}$	source resistance for external oscillator generator		–	–	50	Ω
I and Q amplifiers						
$V_{iIQ(p-p)}$	I and Q channel input voltage (peak-to-peak value)	note 10	–	0.1	–	V
$V_{oIQ(p-p)}$	I and Q channel output voltage (peak-to-peak value)	note 10	–	0.5	–	V
		at 1 dB gain compression; note 10	1.0	–	–	V
IM3	intermodulation distortion in the I and Q channels	note 11	40	–	–	dB
B_{IQ}	bandwidth of I and Q amplifiers	at 0.5 dB	25	–	–	MHz
$\alpha_{ct(IQ)}$	crosstalk between the I and Q channels	note 12	30	–	–	dB
$V_{O(IQ)}$	DC output voltage level for the I and Q amplifier		–	2.45	–	V
$Z_{I(IQ)}$	input impedance of the I and Q channels		–	10	–	k Ω
$Z_{O(IQ)}$	output impedance of the I and Q channels		–	50	–	Ω

Notes to the characteristics

1. Typical supply currents are defined for $V_{CC} = 5\text{ V}$.
2. The I and Q channel output voltages are measured with the following conditions:
 - a) $f_{i(RF)} = \frac{1}{2}f_{i(VCO)} + 500\text{ kHz}$ (70.5 MHz)
 - b) the higher frequencies (140.5 MHz) are filtered out.

3. The I and Q channels gain is defined by $G_{IQ} = \frac{V_{IQ(rms)}}{V_{iRF(rms)}}$.

The gains are measured with the conditions defined in note 2.

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4. The phase and gain error between the I and Q channel outputs is measured as follows:

- a) the oscillator is tuned at $f_{i(VCO)} = 140$ MHz
- b) a sine wave signal $f_{i(RF)} = \frac{1}{2}f_{i(VCO)} + 500$ kHz (70.5 MHz) is applied at the IF input
- c) the higher frequencies (140.5 MHz) are filtered out.

Under these conditions, in each I and Q channel, a sine wave with a frequency of 500 kHz will be present.

These sine waves should be 90 degrees out of phase.

The phase error is defined as the phase quadrature imbalance between the I and Q channels.

The gain error is defined as the gain difference between the I and Q channels.

5. The tilt is defined as the difference between the maximum and the minimum channel gain measured in a frequency band of 25 MHz around $f_{i(RF)}$. The specified tilt is the maximum tilt value found in one of the I or Q channels.
6. The specified noise figure is the maximum value obtained from I and Q channel noise measurement. The noise meter is tuned to 10.7 MHz.
7. The specified intermodulation distortion is the minimum value obtained from intermodulation measurements in the I and Q channels. Intermodulation is measured with two sine wave signals at $f_{i(RF)} = 79$ MHz and $f_{i(RF)} = 81$ MHz with an amplitude of 67 dB μ V for each tone. The difference in level between the converted carriers (9 MHz and 11 MHz) and the intermodulation products after frequency conversion (7 MHz and 13 MHz) is defined as IM3 (see Fig.3).
8. The temperature for the VCO frequency drift is defined for $\Delta T_{amb} = 25$ °C. It is measured in the application circuit of Fig.10 with the following component values for the tank circuit:
 - a) L1: 22 nH (TOKO NE545BNA5 - 100082)
 - b) C1: 15 pF NP0
 - c) C2: 33 pF N220 (220 ppm/°C)
 - d) C3 and C4: 1 nF
 - e) C5: 3.3 μ F
 - f) D1 and D2: BB133
 - g) R1 and R2: 100 k Ω
 - h) R3: 1 k Ω .
9. The phase noise is measured at the oscillator frequency (140 MHz). Due to the frequency divider, the phase noise at the input of the mixers is 6 dB better (111 dBc/Hz at 100 kHz).
10. Output amplifiers are measured separately with an external DC bias applied at pins 9 and 16. The gain is measured for an output signal of 500 mV (p-p) at $f_i = 500$ kHz.
11. The specified intermodulation distortion is the minimum value obtained from intermodulation measurements in the I and Q output amplifier. Intermodulation is measured with two sine wave signals at $f_i = 9$ MHz and $f_i = 11$ MHz at an output level of 500 mV (p-p) for each tone.
12. The crosstalk between the I and Q amplifiers is defined as the ratio between the wanted output signal and the disturbing signal from the other channel. To measure the crosstalk of the I and Q amplifiers, a sine wave 15 MHz, 0.1 V (p-p) is applied at the I input and a sine wave 15.5 MHz, 0.1 V (p-p) is applied at the Q input. For each output, the difference in level is measured between the 15 MHz and the 15.5 MHz component. This difference is the value of the crosstalk between the I and Q amplifiers.

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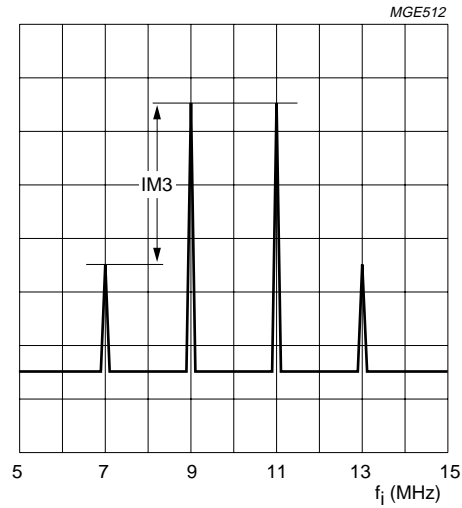


Fig.3 IM3 definition.

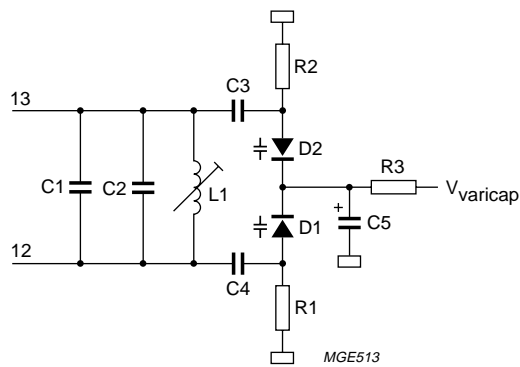
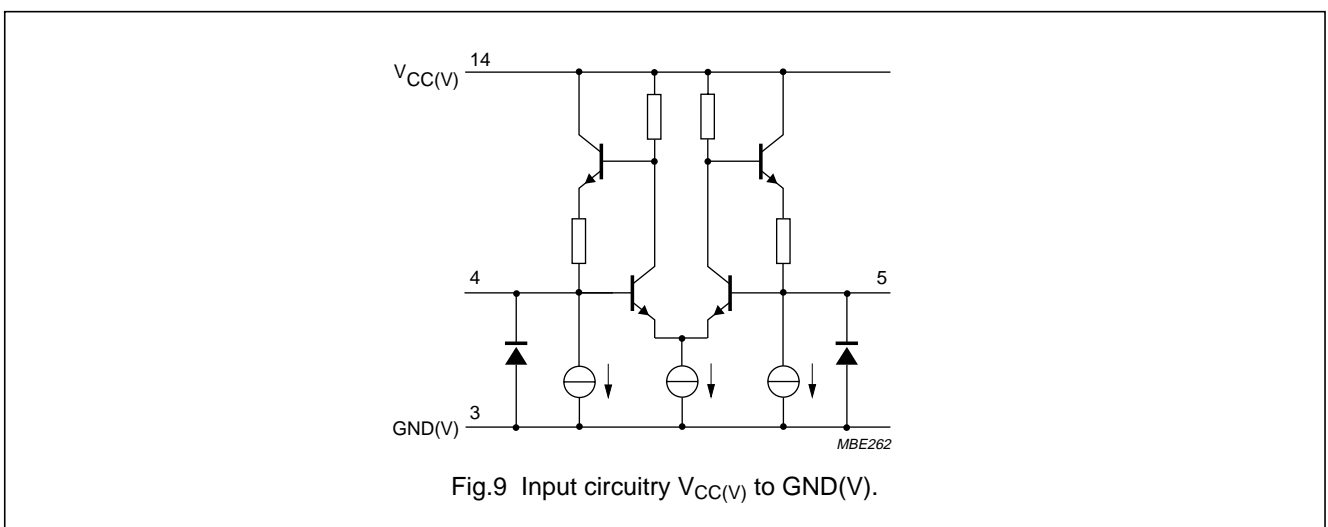
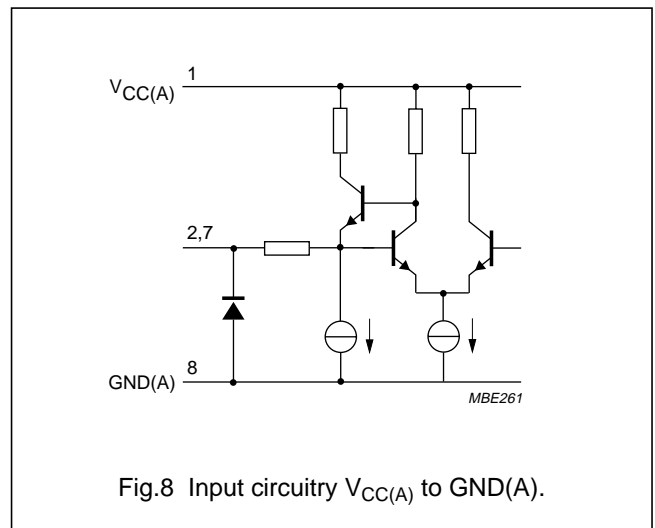
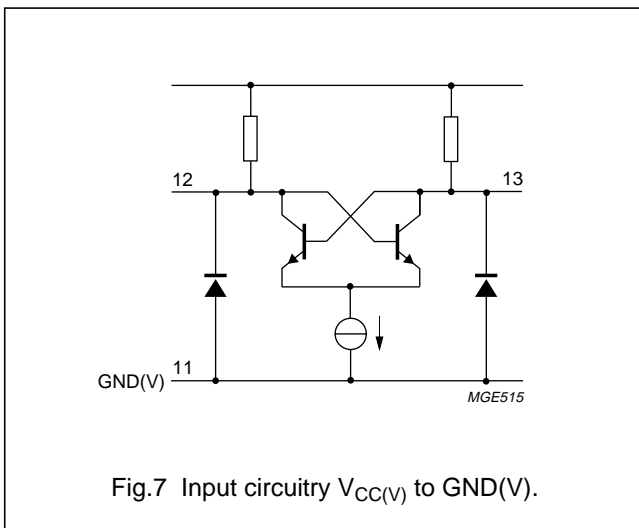
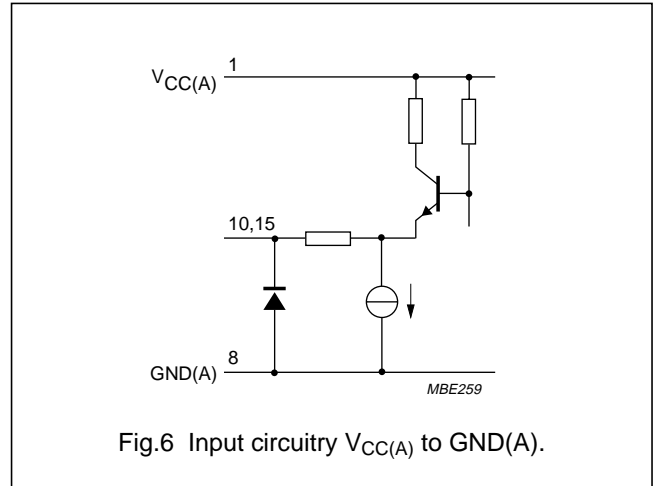
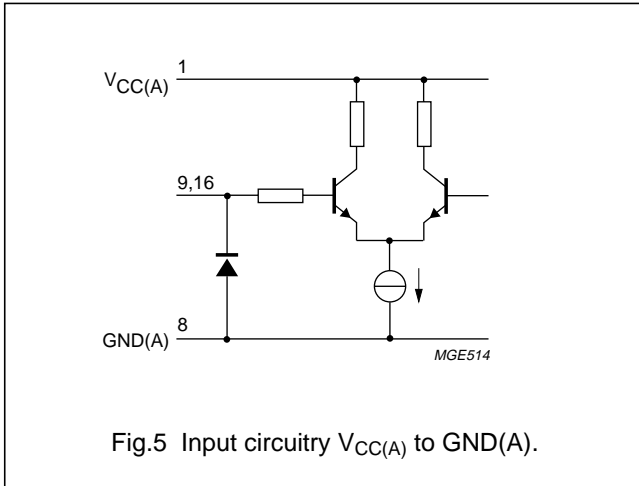


Fig.4 Tank circuit.

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INPUT PIN CONFIGURATION



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APPLICATION INFORMATION

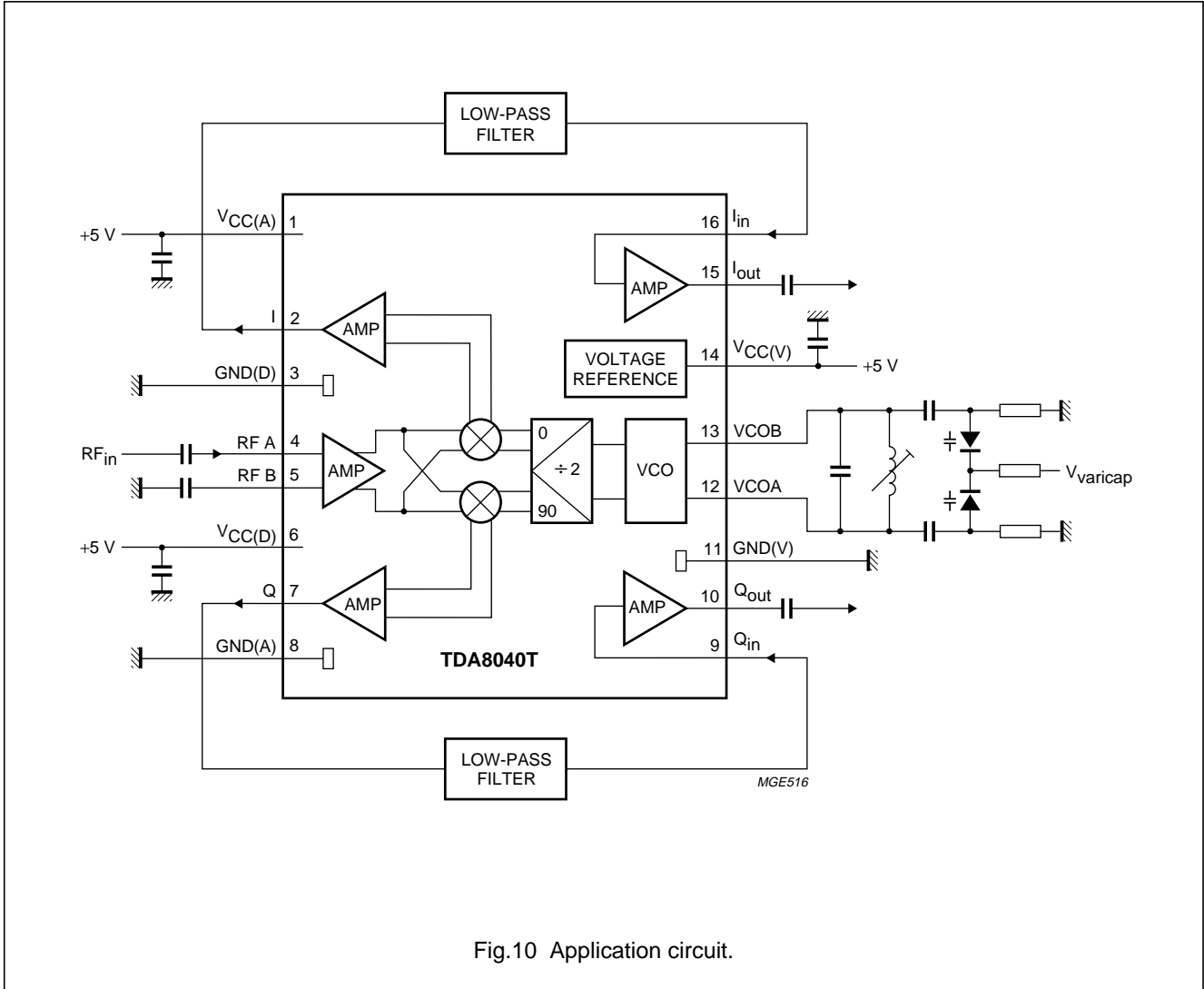


Fig.10 Application circuit.

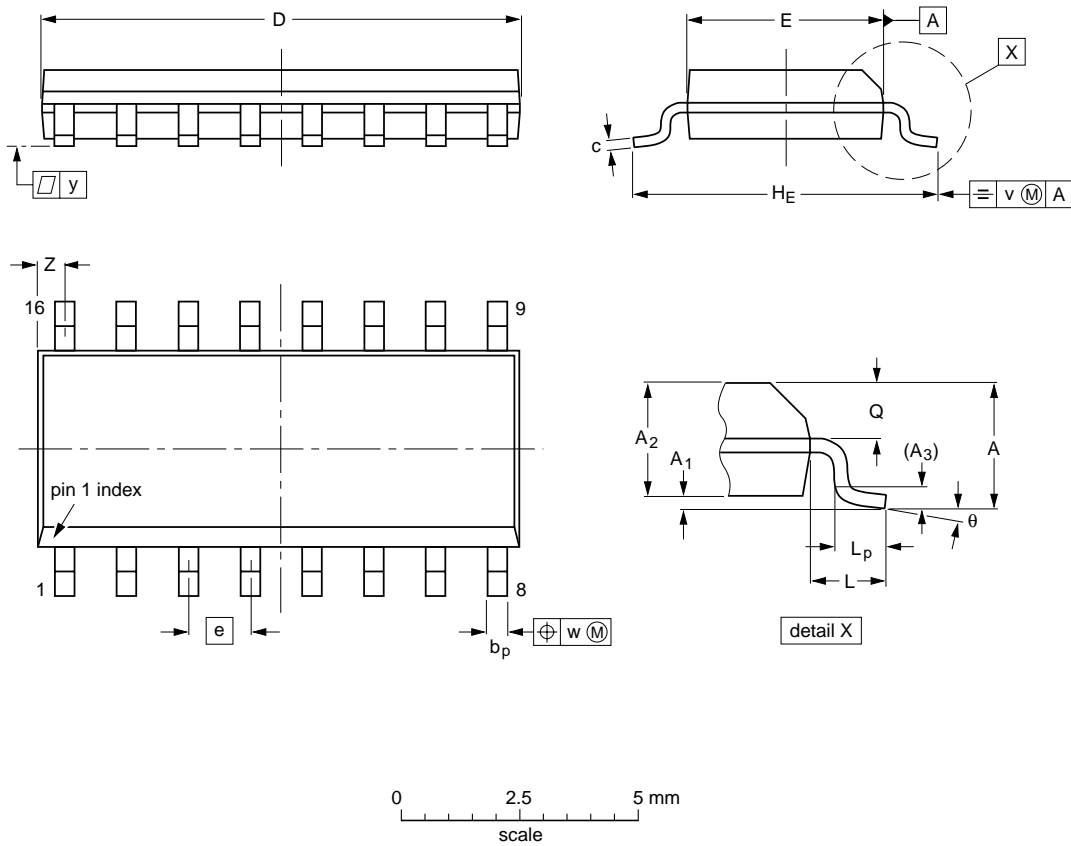
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PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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